*R18 Regulation* *Subject code:* 2P3EC

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

## B.Tech III Semester Regular/Supplementary Examinations, February 2021

## DIGITAL LOGIC DESIGN

**(Computer Science and Engineering)**

***Maximum Marks: 70*** Date:22.02.2021 Duration: 3 hours

**Note:** **1.This question paper contains two parts A and B.**
**2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.**
**3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.**
**4. Each question carries 10 marks and may have a, b, c, d as sub questions.**

## Part-A

**All the following questions carry equal marks** **(10x2M=20 Marks)**

1 State and prove the distributive property of Boolean algebra
2 Write the difference between 1's and 2's complement
3 What is the use of don't care combinations?
4 Draw the logic circuit of a full adder and give its truth table.
5 Compare latch and flip flop
6 Define Register Transfer Language.
7 Explain the functions of an Accumulator
8 Explain following instructions of 8086 microprocessor?
i) ADC ii) AAS
9 Differentiate between PLAs and PALs.
10 Differentiate between RAM and ROM.

## Part-B

Answer All the following questions.**(10MX 5=50Marks)**

11 A. What is gray code? Develop 3 bit gray code for 0 to 7. (5M)
B. i) Simplify A(B+C)+AB+ABC (3M)
ii) Write the truth table and symbols of AND and OR gates. (2M)

OR

12 A. Subtract the following numbers using 2's and 1's complement (5M)
(i) 5250 – 321 (ii) 753 – 864 (iii) 3570 – 2100 (iv) 20 – 1000
B. What are the various logic gates, give the representation along with the truth table. (5M)

13 A. Reduce the following function using K-Map Technique and implement using Universal gate. f(P,Q,R, S) = Σm(0,1,4,8,9,10) + d(2,11) (5M)
B. Implement a full adder with two 4 X1 multiplexers. (5M)

OR

14 A. Design 4 bit Magnitude Comparator and explain in detail. (5M)
B. Implement a full Subtractor circuit with a decoder and two OR gates. (5M)

15 A. What is the drawback of JK flip flop, design a flip flop which overcomes this

drawback and explain with neat diagram. (5M)

B. Design a 4-bit binary ripple counter with D flip-flops. (5M)

OR

16 A. Design 4-bit synchronous counter using JK Flip Flops. (5M)

B. Write short notes on Hazards and Hazard free relations. (5M)

17 A. Explain the following Assembler Directives. (5M)

i) DW ii) DB iii) EQU iv) PROC

B. Explain general purpose and special purpose registers of 8086?(5M)

OR

18 A. Explain following instructions of 8086 microprocessor? (5M)

i) XCHG ii) XLAT iii) IMUL iv) CBW v) INC

B. Explain Flag Register of 8086. (5M)

19 A. Write difference between ROM &PLAs. (5M)

B. Given 32 × 8 ROM with enable input, Show the external connections necessary to construct a 128 × 8 ROM with 4 chips and a decoder. (5M)

OR

20 A. Explain different types ROMs. (5M)

B. Implement the following Boolean functions using PLA with 3 AND gates. (5M)

F1 (ABC) = Σ (3,5,7), F2 = Σ(4,5,7).